

The University of Jordan
School of Engineering
Computer Engineering Department



Academic Year:	2025 / 2026
Semester:	Fall
Course:	0907234 Digital Logic Lab 3 Credits / Dept. Obligatory
Catalog Description:	Introduction to digital logic design tools and hardware programmers. Experiments using simulation and practical implementation of the basic building blocks of a logic using Verilog including basic gates, Encoders, Decoders, Multiplexers. Demultiplexers, Latches, flip flops, registers and counters. In addition to a design project.
Prerequisite(s):	0907231 Digital Logic
Co-requisite(s):	None
Background:	Good background in digital logic concepts.
Textbooks:	<ul style="list-style-type: none">• The lab manual with a set of experiments is posted on the lab website.• Logic and Computer Design Fundamentals, M. Morris Mano and Charles R. Kime, 5th edition, Prentice Hall, 2016..
References:	<ul style="list-style-type: none">• Digital Design: Principles and Practices, Fourth Edition. John F. Wakerly. Prentice Hall, Upper Saddle River, NJ, 2006.• Altera DE2 Development and Education Board User Manual.• A Simple Design in VHDL Using Altera Quartus II 8 Web Edition.
Course Website:	Resources on Microsoft Teams
Schedule & Duration:	14 weeks, 12 sessions, 180 minutes each, including exams.
Student Material:	Textbook, Datasheets, lab handouts, some instructor keynotes, access to a personal computer and internet.
Facilities:	Lab with whiteboard, personal computers, Altera Quartus boards, , oscilloscopes and server.
Course Objectives:	<ul style="list-style-type: none">• The objective of this course is to give hands-on experience on designing, implementing and testing of various logic circuits using discrete components and Verilog HDL.
Course Outcomes and Relation to ABET Program Outcomes:	Upon successful completion of this course, a student should be able to: <ul style="list-style-type: none">• Build and realize basic logic functions from discrete integrated circuits using breadboards [SO1, SO6].• Use modern synthesis tools to build and simulate schematic combinational and sequential logic circuits and deploy them on FPGAs [SO1, SO6].• Use Verilog hardware descriptive language to build, simulate and synthesize decoders, encoders, multiplexors, arithmetic circuits, sequential circuits and

memory units using FPGAs [SO1, SO6].

- Work within a team to formulate, design and simulate a logic circuit based on a formal description [SO1, SO2, SO5].

Lab Schedule:

Week	Date	Activity/Experiment
1	05/10/25	Lab Syllabus and Introduction
2	12/10/25	Exp1. Introduction to Altera and schematic programming
3	19/10/25	Exp2. Introduction to Verilog programming
4	26/10/25	Exp3. Implementation Using Bread boards and Discrete Gates + Quiz
5	02/11/25	Exp4. Decoder/Encoder Applications
6	09/11/25	Exp5. Multiplexers/Demultiplexers Design and Implementation (Time Division Multiplexing)
7	16/11/25	Exp6. Arithmetic Circuits Design and Implementation & Project Assignment
8	23/11/25	Midterm
9	07/11/25	Exp7. Latches and Flip-Flops
10	14/12/25	Exp8. Registers and Counters
11	21/12/25	Open Lab (Project Preparation)
12	28/12/25	Project Discussions
13	12/01/26	Final Exam

Computer Usage:

In-lab computers with Altera software.

Policies:

- Attendance is mandatory and will be recorded each class; university absence rules apply.
- All submitted work must be your own; cheating, plagiarism, unauthorized AI-generated work, or improper use of AI tools will result in academic penalties.
- Professional conduct, timely communication, and adherence to assessment schedules are expected throughout the course.

Assessment Tools & Grading:

<input type="checkbox"/> Midterm Exam (Theory)	0%	<input checked="" type="checkbox"/> Midterm Exam (Practical)	25%
<input checked="" type="checkbox"/> Final Exam	40%	<input checked="" type="checkbox"/> Quizzes	5%
<input type="checkbox"/> Assignments	0%	<input checked="" type="checkbox"/> In-Lab sheets	15%
<input checked="" type="checkbox"/> Projects	15%		
<input type="checkbox"/> Other:			

Instructor(s):

- Eng. Saadeh Sweidan (s.sweadan@ju.edu.jo)
- Eng. Abee Awad (a.awad@ju.edu.jo)
- Eng. Ola Aljalodi (o.jaloudy@ju.edu.jo)

Section(s):

- **Section 1:** Sunday 13:30 – 16:30
- **Section 2:** Monday 10:00 – 13:00
- **Section 4:** Tuesday 13:30 – 16:30
- **Section 5:** Wednesday 13:00 – 16:00
- **Section 6:** Thursday 13:30 – 16:30

Student Outcomes (SO)

- SO1.** An ability to identify, formulate, and solve complex engineering problems by applying principles of engineering, science, and mathematics.
- SO2.** An ability to apply engineering design to produce solutions that meet specified needs with consideration of public health, safety, and welfare, as well as global, cultural, social, environmental, and economic factors.
- SO3.** An ability to communicate effectively with a range of audiences.
- SO4.** An ability to recognize ethical and professional responsibilities in engineering situations and make informed judgments, which must consider the impact of engineering solutions in global, economic, environmental, and societal contexts
- SO5.** An ability to function effectively on a team whose members together provide leadership, create a collaborative and inclusive environment, establish goals, plan tasks, and meet objectives.
- SO6.** An ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.
- SO7.** An ability to acquire and apply new knowledge as needed, using appropriate learning strategies.

Last modified: September 28, 2025